Appl. No. 10/695,476

Amdt. Dated 09/27/2006

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## IN THE CLAIMS

Please cancel claims 48-56 without prejudice.

Please accept a new listing of the pending claims as follows:

- 1 1-37. (Cancelled)
- 1 38. (Previously Presented) A digital integrated
- 2 receiver decoder comprising:
- 3 a plurality of front-ends, including at least a first
- 4 front-end and a second front-end;
- 5 said first front-end being configured to receive a
- 6 first bit stream from a first source and a second front-end
- 7 being configured to receive a second bit stream from a
- 8 second source;
- 9 a transport processor coupled to said first front-end
- 10 and said second front-end, said transport processor being
- 11 configured to process said first bit stream and said second
- 12 bit stream and providing a first processed bit stream and a
- 13 second processed bit stream in response to the first bit
- 14 stream and the second bit stream respectively; and
- 15 at least one decoder coupled to said transport
- 16 processor and configured to simultaneously select the first
- 17 processed bit stream and the second processed bit stream for
- 18 decoding.
- 1 39. (Previously Presented) The digital integrated
- 2 receiver decoder of claim 38, wherein

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- 3 said transport processor is configured to
- 4 simultaneously select the first bit stream and the second
- 5 bit stream for recording.
- 1 40. (Previously Presented) The digital integrated
- 2 receiver decoder of claim 38, wherein
- 3 said first and second front-ends provide outputs to
- 4 first and second demodulators, said first and second
- 5 demodulators each being configured for a different mode of
- 6 demodulation.
- 1 41. (Previously Presented) The digital integrated
- 2 receiver decoder of claim 40, wherein
- 3 said integrated receiver decoder comprises more than
- 4 two front-ends and wherein said transport processor is
- 5 configured to select first and second front-ends and
- 6 wherein each front-end is associated with a differently
- 7 modulated form of input signal.
- 1 42. (Previously Presented) The digital integrated
- 2 receiver decoder of claim 40, wherein
- 3 said transport processor is configured to
- 4 simultaneously select the first bit stream and the second
- 5 bit stream for recording.
- 1 43. (Previously Presented) A digital television
- 2 receiver comprising:
- 3 a plurality of tuners, including at least a first
- 4 front-end and a second front-end;

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- 5 said first front-end being configured to receive a
- 6 first bit stream from a first source and a second front-end
- 7 being configured to receive a second bit stream from a
- 8 second source;
- 9 a transport processor coupled to said first front-end
- 10 and said second front-end, said transport processor being
- 11 configured to process said first bit stream and said second
- 12 bit stream and providing a first processed bit stream and a
- 13 second processed bit stream in response to the first bit
- 14 stream and the second bit stream respectively; and
- 15 at least one decoder coupled to said transport
- 16 processor and configured to simultaneously select the first
- 17 processed bit stream and the second processed bit stream for
- 18 decoding.
- 1 44. (Previously Presented) The digital television
- 2 receiver of claim 43, wherein
- 3 said transport processor is configured to
- 4 simultaneously select the first bit stream and the second
- 5 bit stream for recording.
- 1 45. (Previously Presented) The digital television
- 2 receiver of claim 43, wherein
- 3 said first and second front-ends provide outputs to
- 4 first and second demodulators, said first and second
- 5 demodulators each being configured for a different mode of
- 6 demodulation.
- 1 46. (Previously Presented) The digital television
- 2 receiver of claim 45, wherein
- 3 said digital television receiver includes

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- 4 a plurality of front-ends and
- 5 wherein said transport processor is configured to
- 6 select first and second front-ends and wherein each front-
- 7 end is associated with a differently modulated form of input
- 8 signal.
- 1 47. (Previously Presented) The digital television
- 2 receiver of claim 46, wherein
- 3 said transport processor is configured to
- 4 simultaneously select the first bit stream and the second
- 5 bit stream for recording.
- 1 48-56. (Cancelled).